MAX280
5th Order, Zero DC Error, Lowpass Filter

Manufacturer
Maxim Inc.
http://www.maxim-ic.com

General description
The MAX280 is a 5th-order all-pole instrumentation lowpass filter with no DC error. The filter uses an external resistor and capacitor to isolate the integrated circuit from the DC signal path, thus providing excellent DC accuracy.

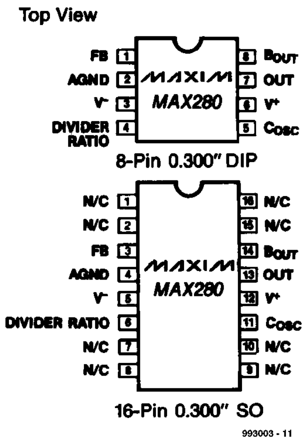
The resistor and capacitor, along with the on-chip 4th-order switched capacitor filter, form a 5th-order lowpass filter. Two MAX280s can be cascaded to form a 10th-order lowpass filter.

The filter cutoff frequency is set by an internal clock which can be externally driven. The clock to cutoff frequency ratio is 100:1, allowing clock ripple to be easily removed.

Application Example
Weather satellite decoder,
Elektor Electronics April 1999.

Features
- Lowpass filter with no DC error
- Low passband noise
- DC to 20 kHz cutoff frequency
- 5th-order all-pole filter
- Internal or external clock
- Cascadable for higher-order rolloff
- Buffered output available
- 8-pin DIP or 16-pin SOIC

Basic operation
Figure 1 illustrates the architecture of the circuit. The output voltage is sensed through an internal buffer, then applied to an internal switched capacitor network which drives the bottom plate of an external capacitor to form a 5th-order lowpass filter. The input and output appear across an external resistor and the IC part of the overall filter handles only the AC path of the signal. The DC offsets of the buffer and the switched capacitor network are blocked by the capacitor and do not



Pin configurations

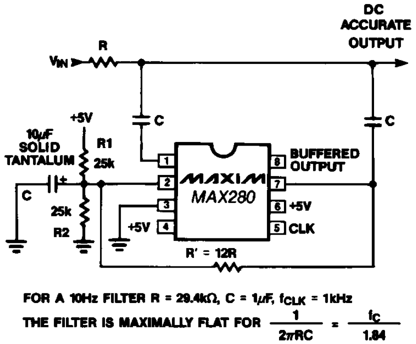
Pin #	Name	Function
1	FB	External capacitor couples to the chip through this pin.
2	AGND	Ground. Connect to the system ground for dual supply operation or mid-supply for single operation. This pin should be well bypassed using a large capacitor for single supply operation.
3	V–	Negatative supply voltage
4	DIVIDER RATIO	The oscillator frequency is divided by either 1, 2 or 4 depending upon the voltage to this pin. This in turn gives a clock to cutoff ratio when tied to V+ of 100:1; when tied to GND of 200:1; and when tied to V– of 400:1.
5	C_{OSC}	Clock input pin for external clock applications. For internal clock operation, connect an external capacitor between this pin and V–.
6	V+	Positive supply voltage
7	OUT	Input to on-chip buffer amplifier
8	B_{OUT}	Output of buffer amplifier

Electrical Characteristics (V+ = +5V, V– = –5V, TA = 25ºC, unless otherwise specified, AC output measured at pin 7, Figure 1)

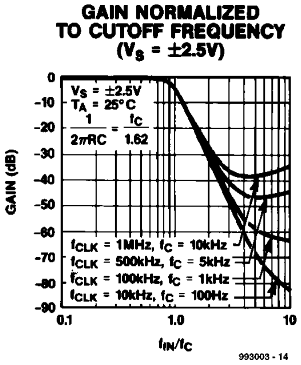
Parameter	Conditions	Min.	Typ.	Max.	Units
Operating Supply Voltage					
Dual Supply		±2.375		±8.0	V
Single Supply		4.75		16.0	
Power Supply Current	C_{OSC} (pin 5 to V–) = 100pF				
	T_A = 25ºC		5.0	7.0	mA
	$T_A = T_{MIN}$ to T_{MAX}		5.0	10.0	
Input Frequency Range			0-20		kHz
Filter Gain at	f_{CLK} = 100kHz, pin 4 at V+ C = 0.01µF, R = 25.78kΩ				
$f_{in} = 0$			0		
$f_{in} = 0.5f_C$ (Note 1)			–0.02	–0.3	dB
$f_{in} = f_C$	$T_A = T_{MIN}$ to T_{MAX}	–2	–3		
$f_{in} = 2f_C$	$T_A = T_{MIN}$ to T_{MAX}	–28	–30		
$f_{in} = 4f_C$	$T_A = T_{MIN}$ to T_{MAX}	–54	–60		
Clock to Cutoff Frequency Ratio f_{CLK}/f_C	f_{CLK} = 100kHz, pin 4 at V+ C = 0.01µF, R = 25.78kΩ	100±1			
Filter gain at fIN = 16kHz	f_{CLK} = 400kHz, pin 4 at V+ C = 0.01µF, R = 6.5kΩ $T_A = T_{MIN}$ to T_{MAX}	–46	–52		dB
f_{CLK}/f_CTempco	Same as above		10		ppm/ºC
Filter Output (pin	Pin 7 buffered with an external opamp, $T_A = T_{MIN}$ to T_{MAX}	±3.5	±3.8		V
Clock Feedthrough			10		mVpp
INTERNAL BUFFER					
Bias Current	TA = 25ºC		2	50	pA
	$T_A = T_{MIN}$ to T_{MAX}		170	1000	
Voltage Swing	R1 = 20kΩ, $T_A = T_{MIN}$ to T_{MAX}	±3.5	±3.8		V
Short Circuit Current Source/Sink			30/2		mA
CLOCK (Note 2)					
Max. Clock Frequency			4		MHz
C_{OSC} Input Sink/Source Current	$T_A = T_{MIN}$ to T_{MAX}		25	80	µA

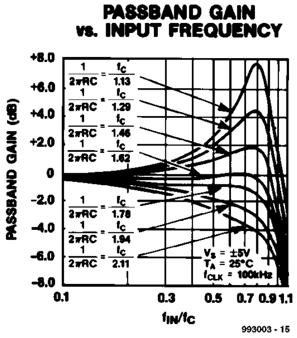
Note 1: f_C is the frequency where the gain is –3dB with respect to the input signal.

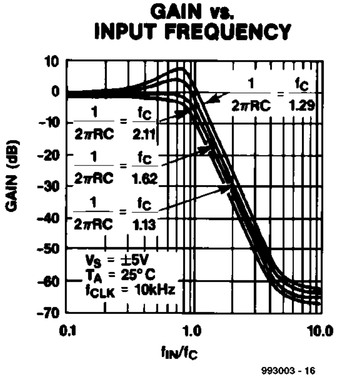
Note 2: The external or driven clock frequency is divided by either 1, 2, or 4 depending upon the voltage at pin 4. When pin 4 = V^+, f_{CLK}/f_C = 100, when pin 4 = GND, f_{CLK}/f_C = 200, pin 4 = $V^–$, f_{CLK}/f_C = 400.

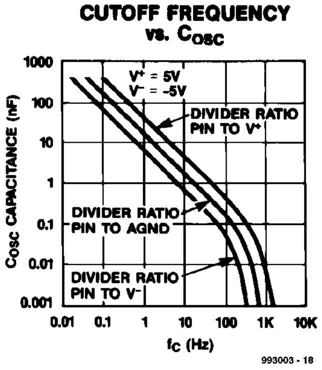


Single 5V supply 5th order LP filter









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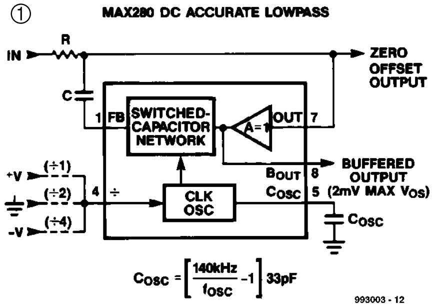


appear at the zero offset output pin.

Use of this external resistor and capacitor also automatically provides the required anti-aliasing filtering for the sampled filter. Further, low frequency noise in the filter IC is attenuated by the external capacitor since any noise at the FB pin goes through a highpass path to the filter output. The filter output pin is unbuffered. This signal can be buffered by the on-chip buffer or by a high accuracy opamp (such as a chopper stabilized opamp) to obtain a buffered DC accurate system. The on-chip buffer has an offset voltage of 2 mV. The offset voltage tempco is typically 1 µV/ºC.

Clock requirements

Using Divider Ratio

DIVIDER RATIO sets the ratio between the internal f_{CLK} (supplied by the MAX280) and f_{OSC} (the output at the DIVIDER RATIO pin). Connect DIVIDER RATIO to V^+ for a 1:1, to GND for a 1:2, and to V^- for a 1:4 f_{CLK}/f_{OSC} ratio.

Using Internal Oscillator

The internal 140 kHz (nominal) oscillator frequency can be modified by connecting an external capacitor in parallel with the on-chip 33pF capacitor, from the C_{OSC} pin to GND (or to V^- if the capacitor is polarized).

The clock frequency can be calculated by:

$$f_{OSC} = 140\text{ kHz }(33\text{pF}/(33\text{pF}+C_{OSC})) \qquad (1)$$

Due to process tolerances, f_{OSC} can vary by ±19.5%. The oscillator frequency can be adjusted by adding a series potentiometer between the capacitor and the C_{OSC} pin. The new frequency can be computed as:

$$f'_{OSC} = f_{OSC}/(1-4RC_{OSC}f_{OSC}) \qquad (2)$$

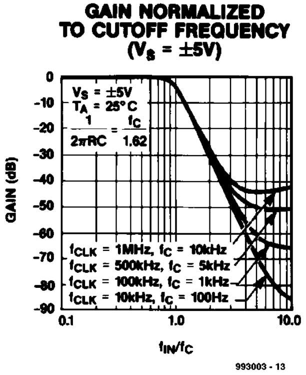
where f_{osc} is the value of the oscillator frequency when R = 0. When an external potentiometer is used, the new value of the oscillator frequency is always higher than the one calculated in Eq. (1). To achieve a wide tuning range, calculate (Eq. 1) the ideal f_{OSC}, C_{OSC} pair, then double the value of C_{OSC} and use a 50k pot to adjust f'_{OSC}. The internal oscillation frequency can be measured directly at the C_{OSC} pin using a low capacitance probe.

Using External Clock

The internal switched capacitor filter requires a clock 100 times higher than the desired cutoff frequency. The external resistor and capacitor is used as part of a feedback loop for the filter and also forms one pole. The internal 4-pole switched capacitor filter is driven by a clock which also determines the filter cutoff frequency. For a maximally flat amplitude response, the clock should be 100 times the desired cutoff frequency and the resistor and capacitor should be chosen such that:

$$(f_C/1.62) = (1/2\pi RC)$$

where f_C is the filter cutoff frequency (–3dB point). Typically R is chosen to be around 20kΩ. For wide temperature range applications, NP0 ceramic capacitors are recommended. Mylar, polystyrene and polypropylene capacitors all provide acceptable performance.


GAIN NORMALIZED TO CUTOFF FREQUENCY (V_S = ±5V)
V_S = ±5V
T_A = 25°C
1/2πRC = f_C/1.62
f_CLK = 1MHz, f_C = 10kHz
f_CLK = 500kHz, f_C = 5kHz
f_CLK = 100kHz, f_C = 1kHz
f_CLK = 10kHz, f_C = 100Hz
GAIN (dB)
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
0.1
1.0
10.0
f_IN/f_C
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